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Request for grant of a patent

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1. Your reference — PAT 02017 GB

2. Patent application number — 0230289.1 — ~~30 DEC 2002~~

3. Full name, address and post code of the or of each applicant

   NOKIA CORPORATION
   Keilalahdentie 4
   02150 Espoo
   Finland

   Patents ADP Number — 07652217003

   If the applicant is a corporate body, give the country/state of its incorporation — Finland

4. Title of the invention — Improved phase locked loop

5. Name of your agent
   "Address for service" in the United Kingdom to which all correspondence should be sent

   Nokia IPR Department
   Nokia House, Summit Avenue
   Farnborough, Hants
   GU14 ONG
   7577638001

   Patents ADP number — 07577638001

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and the or each application number

Country	Priority Application Number	Date of Filing

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of Filing

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? (Answer 'Yes' if:

   a) any applicant named in part 3 is not an inventor, or
   b) there is an inventor who is not named as an applicant, or
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   Yes

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Description	10
Claims(s)	4
Abstract	—
Drawing(s)	3

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Priority documents

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Statement of inventorship and right to grant of a patent (Patents Form 7/77)

Request for preliminary examination and search (Patents Form 9/77)

Request for substantive examination (Patents Form 10/77)

Any other documents (please specify)

11. I/We request the grant of a patent on the basis of this application.

Signature [signature] Date 30/12/2002

James Seymour

12. Name and daytime telephone number of person to contact in the United Kingdom

James Seymour 01252 867249

PAT 02017 GB

IMPROVED PHASE LOCKED LOOP.

Embodiments of the present invention relate to phase locked loops.

Fig. 1 illustrates a phase locked loop (PLL) 10. The PLL comprises in order: a reference oscillator 12, a reference counter 14, a phase detector 16, a loop filter 18, a voltage controlled oscillator 20, and a feedback loop 22 from the VCO 20 through a loop counter 24 to the phase detector 16.

Reference oscillator supplies a reference frequency signal 21, having a frequency Fref, to the reference counter 14. The reference counter operates as a divider and produces an output pulse when it has counted M input pulses of the reference frequency signal 21. The value of M can be varied via an input control signal 23. Thus the first counter produces a reduced frequency input signal 25 which has a frequency 1/M Fref.

The phase detector 16 receives the reduced frequency input signal 25 at one input and a reduced frequency output signal 27 at the other input. The output signal 29 from the phase detector passes through the loop filter 18 to provide an input voltage signal 31 to the VCO 20. The loop filter is generally a series combination of resistor and capacitor connected from a node, in the connection between the phase detector 16 and the VCO 20, to ground. The VCO 20 converts the input voltage signal 31 to an oscillating output signal 33 at frequency Fout.

The oscillating output signal 33 is fed to loop 22, where it is input to the loop counter 24. The loop counter 24 operates as a divider produces an output pulse when it has counted N input pulses of the oscillating output signal 33. The value of N can be varied via an input control signal 35. Thus the second counter provides as a second input to the phase detector 16, a reduced frequency output signal 27 which has a frequency 1/N Fout.

When the reduced frequency output signal 27 lags the reduced frequency input signal 27, the phase detector 16 sinks current to the loop filter 18 and the voltage input to the VCO 20 rises. The VCO 20 increases the frequency Fout of the oscillating output signal 33 and the reduced frequency output signal, which reduces the lag.

When the reduced frequency output signal 27 leads the reduced frequency input signal 27, the phase detector 16 sinks current from the loop filter 18 and the voltage input to the VCO 20 drops. The VCO 20 decreases the frequency Fout of the oscillating output signal 33 and the reduced frequency output signal, which reduces the lead.

Consequently, the loop moves towards 'lock' at which Fout = Fref * N/M

Such phase locked loops suffer from a number of problems. One problem is a long settling time after a change in frequency which may make it unsuitable modern multi-slot communication systems. Another problem is that there is an inherent frequency overshoot during a frequency change and the VCO must consequently have a large operational frequency range and may therefore introduce phase noise.

It would be desirable to provide an improved phase locked loop.

According to one aspect of the present invention there is provided a phase locked loop circuit, for providing an oscillating output signal at an output frequency, comprising: a reference counter; a loop counter; a phase detector having a first input coupled to the reference counter and a second input coupled to the loop counter; a voltage controlled oscillator having an input coupled to the output of the phase detector and an output for providing the oscillating output signal;
a feedback loop coupling the output of the voltage controlled oscillator to the input of the loop counter; and delay circuitry arranged to introduce a discrete delay into the output of the loop counter and/or the reference counter.

The delay circuit may additionally comprise a variable delay component for introducing a continuously variable delay into the output of the loop counter and/or the reference counter.

A capacitor is connected between the phase detector and the voltage controlled oscillator; there is no loop filter. The reduced capacitance results in an improved settling time.

According to another aspect of the present invention there is provided a method of changing the frequency of an oscillating output signal comprising the steps of: adapting

the reference counter and/or the loop counter of a phase locked loop; and introducing a discrete delay into the output of the loop counter and/or the reference counter.

The method may also have the step of introducing a continuously variable delay into the output of the loop counter and/or the reference counter. A temporary variation of the discrete delay may result in a corresponding permanent variation in the variable delay.

According to a further aspect of the present invention there is provided a frequency synthesiser, for providing an oscillating output signal at an output frequency, comprising frequency compensation means arranged to maintain the output frequency and phase delay means arranged to vary discretely the phase of an input signal provided to the compensation means.

The phase delay means may additionally continuously vary the phase delay of the first input signal or, as an alternative, the second input signal.

Embodiments of the invention reduce any frequency over shoot when the output frequency is change. This allows voltage controlled oscillators of reduced range to be used.

The use of both variable delay and discrete delay, allows the introduction of a large delay without having to have a mechanism for introducing a large continuous delay. The variable delay component can therefore operate over a reduced range, which means that it can have a reduced sensitivity and therefore is less susceptible to introducing phase noise.

For a better understanding of the present invention reference will now be made by way of example only to the accompanying drawings in which:

Fig1 illustrates a prior art phase locked loop;

Fig 2 illustrates an adapted phase locked loop according to one embodiment of the present invention;

Fig 3 is an example of one possible signal timing diagram for the phase locked loop of Fig 2;

Fig. 4 illustrates an adapted phase locked loop according to a second embodiment of the present invention.

Fig 2 illustrates an adapted phase locked loop (PLL) 100 with a delay locked loop (DLL) wrapped around the phase detector 16.

The adapted PLL 100 differs from the PLL 10 of Fig. 1 in that:
a) it does not have a loop filter between the phase detector 16 and the VCO 20, but instead has a capacitor 102 connected between a node 104, between the phase detector 16 and the VCO 20, and ground.
b) it additionally has a variable delay component 106 connected between the first counter 14 and the phase detector 16
c) it has a delay locked loop (DLL) 110 wrapped around the phase detector 16. The DLL takes an input from the node 104 and provides a first delay control signal 121 to the reference counter 14 and provides a second delay control signal 114 to the variable delay component 106.

The adapted phase locked loop (PLL) 100 comprises in order: the reference oscillator 12, the reference counter 14, the variable delay component 106, the phase detector 16, a capacitor 102, a negative feed-back loop from the capacitor 102 to the variable delay component 106 and the first counter 14, that completes the DLL 110, a voltage controlled oscillator 20, and a negative feedback loop 22 from the VCO 20 output through the loop counter 24 to the phase detector 16, that completes the PLL.

The reference oscillator 12 supplies a reference frequency signal 21 to the reference counter 14. The reference counter 14 keeps a counter value m which is incremented once for each received pulse of the reference frequency signal 21. When the counter value m equals a programmed value M, the reference counter 14 produces an output pulse and the counter value m is reset to zero. The reference counter divides the frequency of the reference signal 21 by M. The value of M is programmed via the first input control signal 23.

The value of m can be controlled by the first delay control signal 121. A variation of m produces a temporary compensation in the frequency of the signal produced by the reference counter 14. The compensation of the frequency only lasts for one pulse cycle because M is not varied and is therefore 'temporary'. The reference counter 14 can therefore be controlled to introduce delays in a discrete manner. The delayed signal

output by the reference counter, the partially compensated signal 123, is further delayed by the variable delay component 106 to produce a fully compensated signal 125, which is input to the phase detector 16.

The variable delay component adds a continuously variable delay to the partially compensated signal 123 to create the fully compensated signal 125. The value of the continuously variable delay is controlled by a second input control signal 115 from the DLL 110.

The reference counter 14 provides, gross or coarse variations in the delay in a digital all or nothing manner. The variable delay component provides an analogue variation of the delay which can be used for fine tuning. The presence of a mechanism for introducing gross delays enables the delay range of the variable delay component and therefore it sensitivity to be limited. This reduces phase noise.

The phase detector 16 receives the fully compensated signal 125 at a first input and a reduced frequency output signal 27 at the second input. The output signal 29 from the phase detector provides an input voltage signal 31 to the VCO 20. The VCO converts the input voltage signal 31 to an oscillating output signal 33 at frequency Fout.

The oscillating output signal 33 is fed to loop 22, where it is input to the second counter 24. The second counter produces a reduced frequency output signal 27 which has a frequency 1/N Fout.

When the reduced frequency output signal 27 lags the fully compensated signal 125, the phase detector 16 sinks current to the capacitor 102 and the voltage input to the VCO 20 rises. The VCO 20 increases the frequency Fout of the oscillating output signal 33 and the reduced frequency output signal 27, which reduces the lag.

When the reduced frequency output signal 27 leads the fully compensated signal 125, the phase detector 16 draws current from the capacitor 104 and the voltage input to the VCO 20 drops. The VCO 20 decreases the frequency Fout of the oscillating output signal 33 and the reduced frequency output signal 27, which reduces the lead.

The DLL 110 comprises: a high input impedance buffer 112; a subtractor 114; a detector

116; a logic controller 118; a gross delay counter 120; and a digital to analogue converter (DAC) 122.

The high input impedance buffer 112 is connected to node 104 and receives as an input the input voltage signal 31 that is also provided to the VCO 20. The high impedance buffer is a simple op amp follower which presents a high impedance to node 104.

The subtractor 114 receives from the high impedance buffer 112 a buffered voltage signal 113 and subtracts from it an output analogue signal 123 from the DAC 122, to produce the second input control signal 115 that is provided as an input to the variable delay component 106.

The detector 116 is connected to the output of the subtractor 114. It detects when the second input control signal 115 exceeds any one of a plurality of programmed thresholds. The detector provides a detection signal 117 to the logic controller 116 when a threshold is exceeded indicating that threshold.

The logic controller 118 responds to the detection signal 117 to produce a first input control signal 121 that is provided to the first counter 14 and a corresponding counter control signal 119 that is provided to the gross delay counter 120. The value of the gross delay counter 120 is converted from a digital to an analogue value by the DAC 122 and provided as the output signal 123 to the subtracting input to the subtractor 114.

The DLL 110 operates as a feed-back loop to control the delay introduced by the reference counter 14 and variable delay component 106.

The frequency of the oscillating output signal 33 is generally changed by reprogramming the value of N in the loop counter 24.

If N is increased, the reduced frequency output signal 27 starts to lag the fully compensated signal 125 and the voltage 31 increases, which increases Fout. The increasing input voltage signal 31 increases the second input control signal 115. This introduces a positive delay into the fully compensated signal 125 via the variable delay component 106. Consequently, the amount by which the reduced frequency output signal 27 lags the fully compensated signal 125 is reduced. If the value of the introduced delay

represented by the second input control signal 115 is below a threshold, then the reference counter 14 is unaffected. If the value of the introduced delay exceeds a threshold, the detector 116 detects this and informs the logic controller 118. The logic controller 118 then provides a first input control signal 121 to the reference counter 14. The signal 121 represents a number x of reference clock cycles of duration *t*. The value of x is a natural number dependent upon the threshold that has been exceeded, or the particular threshold that has been exceeded if there are multiple upper thresholds of different values. The duration x * *t* is such that the delay introduced via the variable delay component 106 by the second input control signal 115 is brought within the exceeded threshold.

The reference counter subtracts the value x from its current value of its counter value m. This introduces a delay of x * t via the reference counter 14.

The signal 119 is the same as the first input control signal 121. The gross delay counter 120 is incremented by the value x. The counter therefore holds the total number of reference clock cycles of delay that have been introduced by the signal 121 via the reference counter 14. The DAC 122 converts the counter value of the gross delay counter 120 to an analogue output signal 123 which is then subtracted from the buffered voltage signal 113 to reset the second control signal 115. The new value of the second input control signal resets the variable delay component so that the delay introduce by it is reduced by x * *t*. This brings the delay introduced via the variable delay component 106 by the second input control signal 115 beneath the detected threshold.

Fig. 3 illustrates a signal timing diagram for the partially compensated signal 123, the VCO input voltage signal 31, the fully compensated signal 125 and the second input control signal 115.

The value of N is increased at time T1. At T1 frequency output signal 27 begins to lag the fully compensated signal 125. The input voltage signal 31 rises and the variable delay component introduces an increasing delay, dependent upon the input voltage signal 31. At time T2 the second input control signal 115 exceeds an upper threshold. As a consequence a gross delay equivalent to one reference clock cycle is introduced into the reference counter 14 and the delay introduced by the variable delay component 106 is reduced by the same amount by reducing the second input control signal 115. The

introduction of the gross delay, equivalent to one reference clock period, into the partially compensated signal 123 can be observed at time T3. The DLL acts directly on the phase and removes the phase error, by adjusting the delay, extremely quickly.

If N is decreased, the reduced frequency output signal 27 starts to lead the fully compensated signal 125 and the voltage 31 decreases, which decreases Fout. The decreasing input voltage signal 31 decreases the second input control signal 115. This introduces a negative delay (a phase advance) into the fully compensated signal 125 via the variable delay component 106. Consequently, the amount by which the reduced frequency output signal 27 leads the fully compensated signal 125 is reduced. If the value of the introduced delay represented by the second input control signal 115 does not exceed a threshold, then the reference counter 14 is unaffected. If the value of the introduced delay exceeds a threshold, the detector 116 detects this and informs the logic controller 118. The logic controller 118 then provides a first input control signal 121 to the reference counter 14. The signal 121 represent a number -y of reference clock cycles of duration *t*. The value of y is a natural number dependent upon the threshold that has been exceeded, or the particular threshold that has been exceeded if there are multiple lower thresholds of different values. The duration -y * *t* is such that the delay, introduced via the variable delay component 106 by the second input control signal 115, is brought within the exceeded threshold.

The reference counter adds the value y to its current value of its counter value m. This introduces a phase advance of y * t via the reference counter 14.

The signal 119 is the same as the first input control signal 121. The gross delay counter 120 is decremented by the value y. The counter therefore holds the total number of reference clock cycles of delay that have been introduced by the signal 121 via the reference counter 14. The DAC 122 converts the counter value of the gross delay counter 120 to an analogue output signal 123, which is then subtracted from the buffered voltage signal 113 to reset the second control signal 115.

It will therefore be appreciated that the variable delay component operates within thresholds defined by the detector 116, which may be programmed.

In the embodiment of Fig. 2, the DLL 110 wraps around the phase detector 16 with an

input to the reference path. The variable delay component 106 is placed in the reference path between the reference counter 14 and the phase detector 16. The DLL 110 provides an input to the reference counter 14 and the variable delay component 106.

It is also possible to arrange the DLL 110 so that it wraps around the phase detector 16 with an input to the loop path of the PLL 100 as illustrated in Fig. 3. The variable delay component 106 is placed in the loop path between the loop counter 24 and the phase detector 16. The DLL 110 provides an input to the loop counter 24 and the variable delay component 106. When the delay is introduced into the loop path, the sense in which delays are added at the variable delay component 106 and the loop counter 24 is opposite to that when the delay is introduced into the reference path.

The variable delay component comprises a comparator and a linear ramp generator. The output of the comparator provides the fully compensated signal 125. One input to the comparator is the second control signal 115 and the other is from the linear ramp generator. The liner ramp generator comprises a transistor and a capacitor connected in parallel between the input node to the comparator and ground. The input node is also connected to a series connected resistor and inductor, which provides a constant current source. The transistor receives the partially compensated signal 123 as a switching input. When the transistor is switched on there is a low resistance path to earth via the transistor and current flows through the resistor and inductor series to earth. When the transistor is switched off there is a high resistance path to earth and the current flowing through the inductor and resistor series combination charges the capacitor connected in parallel with the transistor. When the voltage developed by this capacitor exceeds the second input control signal 115 value, the output of the comparator, the compensated signal 125, switches.

In the combination of the adapted PLL 100 and DLL 110, the PLL sets the frequency and the DLL 110 sets the phase. The presence of delay locked loop introduces a zero which allows the conventional loop filter of a PLL to be replaced with the capacitor. Thus conventional loop filter of a PLL includes a large valued capacitance and a resistor connected in series from node to ground is replaced by a small value capacitor. The small value of the capacitor provides a very fast settling time after a frequency step is performed.

In the above described embodiments the discrete phase compensation by the counter occurs before the variable phase compensation by the variable delay component. That is the variable delay component follows the counter. In other embodiments, the variable delay component may precede the counter so that the variable phase compensation occurs before the discrete phase compensation.

In the above described embodiments, the DLL and the PLL share the same phase detector. In other embodiments, the DLL may have its own phase detector and the PLL may have its own phase detector.

By adjusting the thresholds at which detector 116 operates, large variations in phase delay can be achieved using a variable delay component with a limited range (and sensitivity). This reduces phase noise.

Although the embodiments of the invention have been described with reference to an integer PLL, it may also be used in fractional PLLs.

It should be appreciated that the adapted LL described above has many application, such as controlling the transmission or receiving frequency of a radio transceiver. It may for example, be used as a frequency synthesiser to provide a carrier signal for modulation or provide a frequency or phase modulated signal.

Although embodiments of the present invention have been described in the preceding paragraphs with reference to various examples, it should be appreciated that modifications to the examples given can be made without departing from the scope of the invention as claimed.

Whilst endeavouring in the foregoing specification to draw attention to those features of the invention believed to be of particular importance it should be understood that the Applicant claims protection in respect of any patentable feature or combination of features hereinbefore referred to and/or shown in the drawings whether or not particular emphasis has been placed thereon.

Claims

1. A phase locked loop circuit, for providing an oscillating output signal at an output frequency, comprising:
a reference counter;
a loop counter;
a phase detector having a first input coupled to the reference counter and a second input coupled to the loop counter;
a voltage controlled oscillator having an input coupled to the output of the phase detector and an output for providing the oscillating output signal;
a feedback loop coupling the output of the voltage controlled oscillator to the input of the loop counter; and
delay circuitry arranged to introduce a discrete delay into the output of the loop counter and/or the reference counter.

2. A phase locked loop circuit as claimed in claim 1, wherein the delay circuit temporarily introduces an off-set into the loop counter and/or the reference counter.

3. A phase locked loop circuit as claimed in claim 1 or 2, wherein the delay circuit comprises a variable delay component for introducing a continuously variable delay into the output of the loop counter and/or the reference counter.

4. A phase locked loop circuit as claimed in claims 3, wherein the delay circuitry comprises a detector for detecting when the variable delay component exceeds a threshold and control means for introducing a discrete delay in response to said detection.

5. A phase locked loop circuit as claimed in claim 3 or 4, wherein the delay circuit is arranged to compensate a variation in the discrete delay with a variation in the variable delay.

6. A phase locked loop circuit as claimed in claim 3, 4 or 5, wherein the delay circuitry is arranged such that a maximum variable delay is substantially equal to a minimum discrete delay.

7. A phase locked loop circuit as claimed in any one of claims 3 to 6, wherein the delay circuitry comprises a feedback loop which provides an input to the variable delay component that is dependent upon both the voltage at the input to the voltage controlled oscillator and the discrete delay introduced into the loop counter and/or the reference counter.

8. A phase locked loop circuit as claimed in claim 7, wherein the delay circuit temporarily introduces an off-set into the loop counter and/or the reference counter and comprises: a summation means for summing the introduced offsets; a digital to analogue conversion means for converting the total introduced offset into an analogue signal representing the total introduced discrete delay; and subtraction means for subtracting the analogue signal from a signal representative of the voltage at the input of the voltage controlled oscillator to produce the input to the variable delay component.

9. A phase locked loop circuit as claimed in any preceding claim, further comprising a capacitor connected between the phase detector and the voltage controlled oscillator.

10. A phase locked loop circuit as claimed in claim 9, wherein the phase detector output is coupled to the input of the voltage controlled oscillator without an intervening loop filter.

11. A frequency synthesiser comprising a phase locked loop circuit as claimed in any preceding claim.

12. A method of changing the frequency of an oscillating output signal comprising the steps of:
adapting the reference counter and/or the loop counter of a phase locked loop; and
introducing a discrete delay into the output of the loop counter and/or the reference counter.

13. A method as claimed in claim 12 further comprising the step of introducing a continuously variable delay into the output of the loop counter and/or the reference counter.

14. A method as claimed in claim 13, wherein a temporary variation of the discrete delay

results in a corresponding permanent variation in the variable delay.

15. A frequency synthesiser, for providing an oscillating output signal at an output frequency, comprising:
frequency compensation means arranged to maintain the output frequency; and phase delay means arranged to vary discretely the phase of an input signal provided to the compensation means.

16. A frequency synthesiser as claimed in claim 15, wherein the compensation means comprises: an input for receiving a first input signal; comparison means for comparing the first input signal and a second input signal; control means for controlling the output frequency in dependence upon the comparison; and a negative feedback loop for providing the second signal as an input to the compensation means.

17. A frequency synthesiser as claimed in claim 16, wherein the comparison means is a phase detector.

18. A frequency synthesiser as claimed in claim 16 or 17, wherein the control means comprises a capacitor, a voltage controlled oscillator having its input connected to the capacitor and means for sourcing and sinking current to said capacitor and thereby control the output of said voltage controlled oscillator and the output frequency.

19. A frequency synthesiser as claimed in any one of claims 16, 17 or 18, wherein the negative feedback loop comprises programmable means for adjusting the second input signal.

20. A frequency synthesiser as claimed in claim 19, wherein the programmable means is a counter.

21. A frequency synthesiser as claimed in any one of claims 15 to 20, wherein the phase delay means is additionally arranged to continuously vary the phase delay of the first input signal.

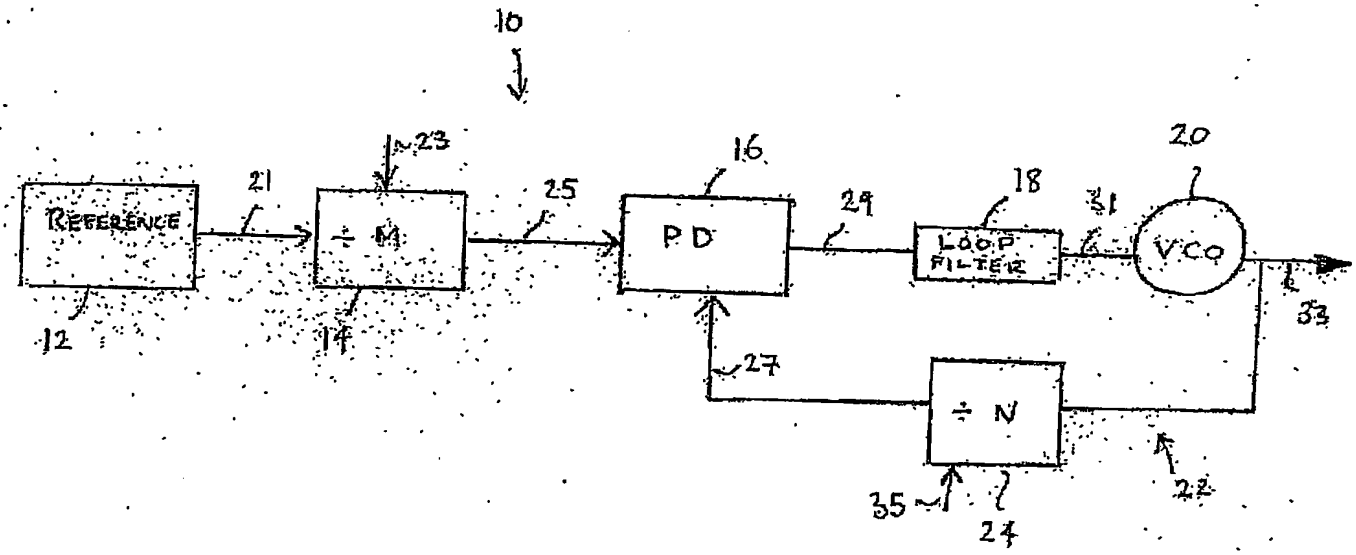
22. A frequency synthesiser as claimed in any one of claims 15 to 20, wherein the phase delay means is additionally arranged to continuously vary the phase delay of the second

input signal.

23. A frequency synthesiser as claimed in claim 21 or 22, wherein the phase delay means comprises a negative feedback loop.

24. A phase locked loop substantially as hereinbefore described with reference to and/or as shown in the accompanying Figs. 2, 3 and 4.

25. Any novel subject matter or combination including novel subject matter disclosed, whether or not within the scope of or relating to the same invention as the preceding claims.


10
REFERENCE
÷ M
PD
LOOP FILTER
VCO
÷ N
12
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23
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29
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33
35
24
22

Fig 1

2/3

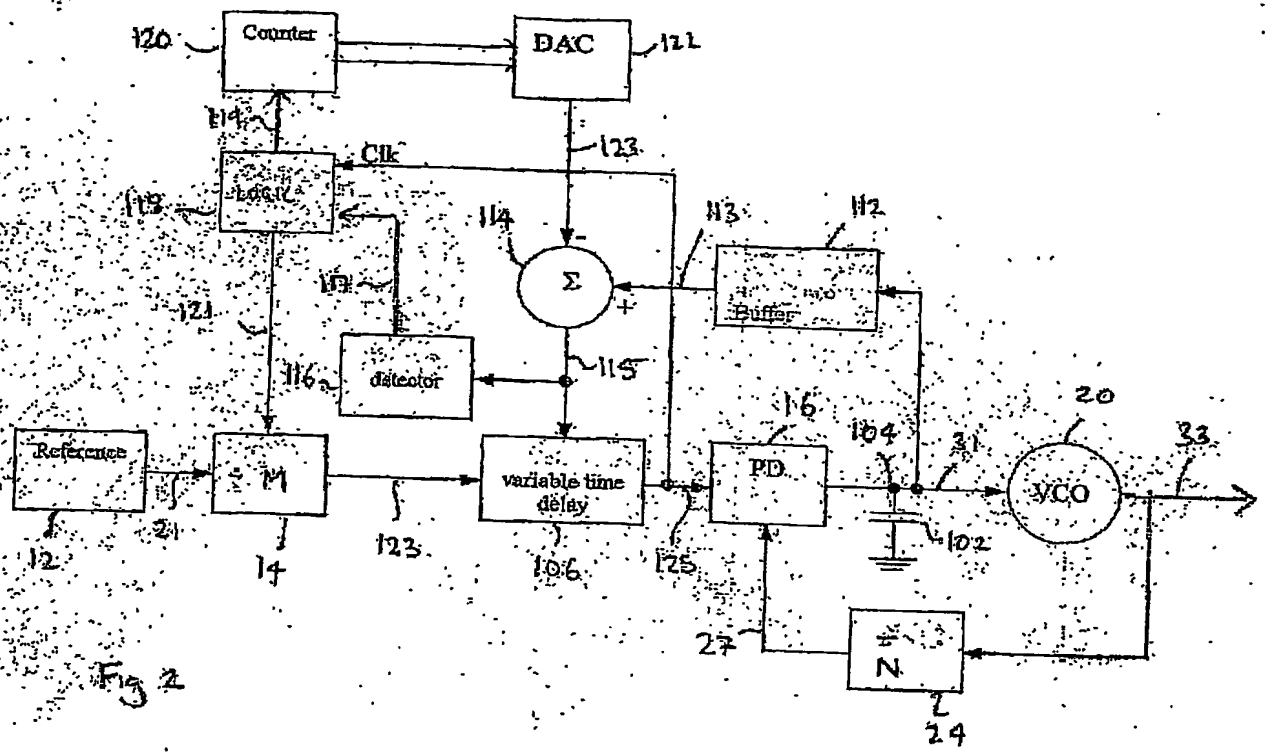

Fig 2

Signal timing diagram

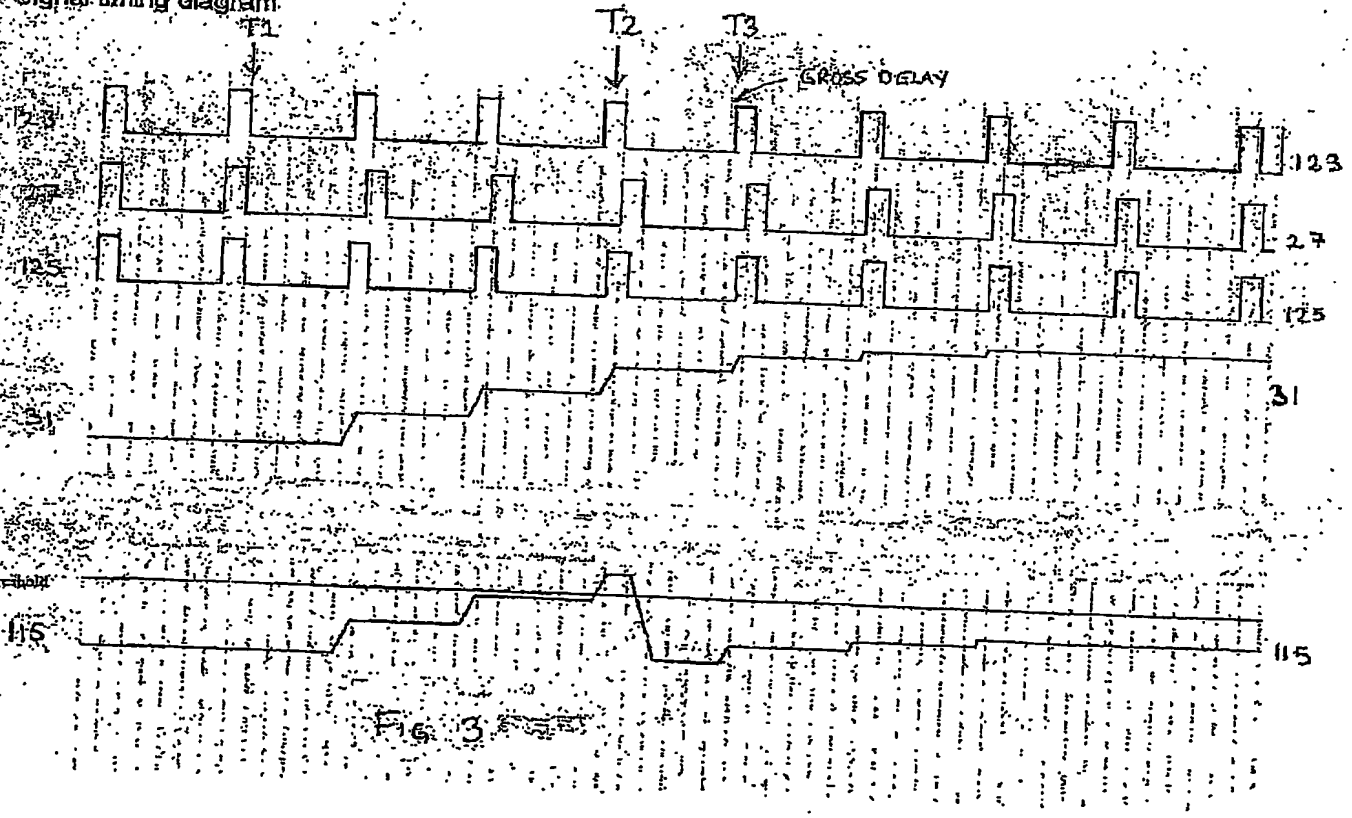

Fig 3

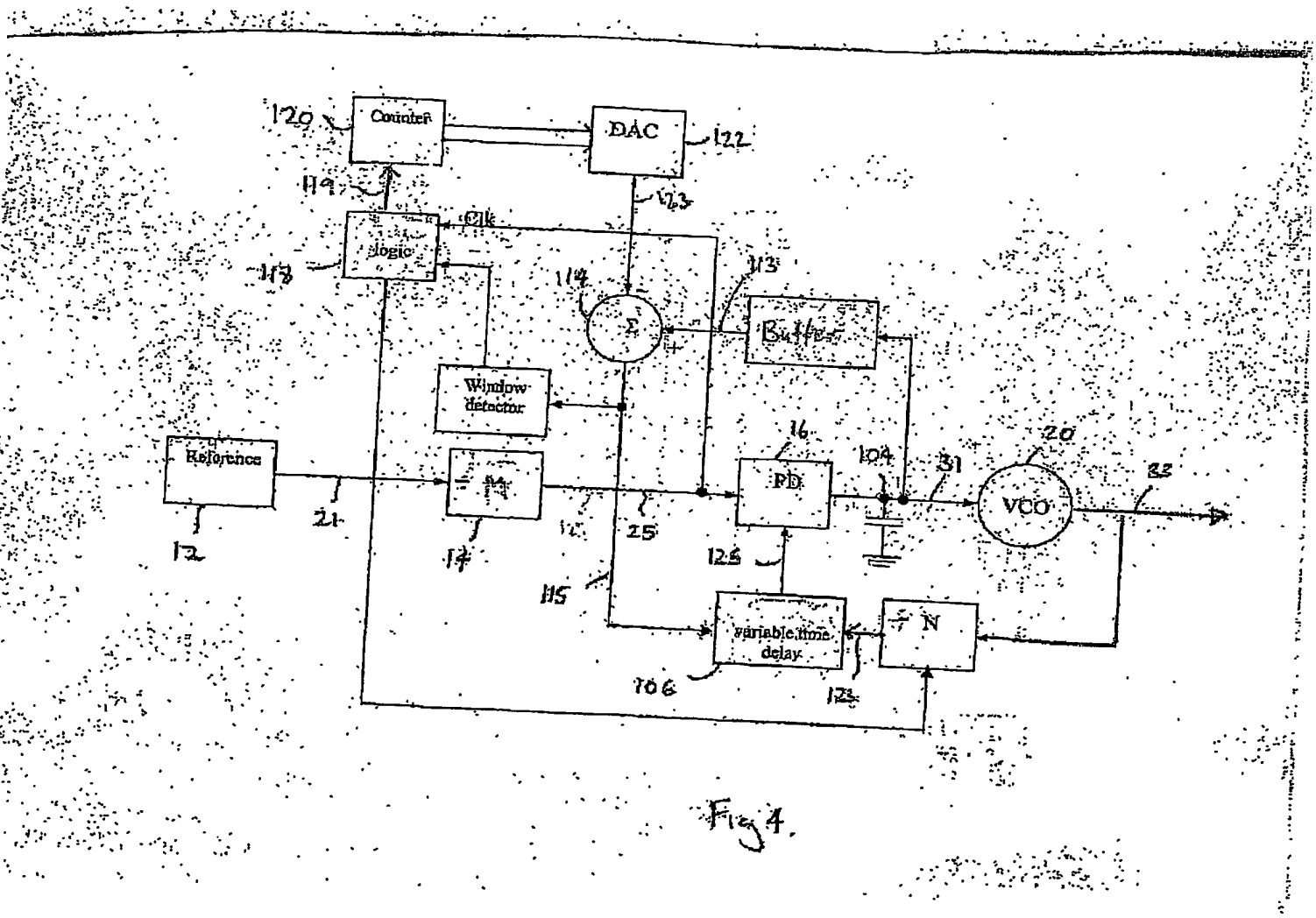
120
Counter
DAC
122
119
123
Clk
logic
118
114
113
Σ
Buffer
Window detector
16
104
20
31
32
Reference
M
PD
VCO
21
12
14
25
126
115
variable time delay
N
106
123

Fig 4.